

REMARKS/ARGUMENTS

Claim Rejections - 35 USC § 102(e)

Claims 1, 5, 9 and 11-13 were rejected under 35 U.S.C. 102(e) as being anticipated by Kean (U.S. Patent No. 7,203,842).

Claims 1, 5, 9, from the last Amendment, are cancelled. The reason for rejection no longer applies. Claims 1, 5, 9, as amended, correspond to the Claims 3, 7, 10, respectively, from the last Amendment, and are addressed in the 103 rejection section below. Claim 11 which depends on the amended Claim 9 is also addressed below.

Regarding Claim 12 – 13, Applicants respectfully submit the conclusion stated in the Office Action of Oct. 10, 2007 is incorrect. Claim 12 has a limitation about the root key random number to seed a random number for a session key that is not taught nor suggested by Kean. Moreover, Kean does not teach root key and session keys altogether because Kean has a standalone memory chip only, a FPGA, that is transferring data to elsewhere; nothing related to the system is on the FPGA. Claim 13 depends on Claim 12. Claims 12 and 13 are therefore believe allowable over Kean.

Claim Rejections - 35 USC § 103

Claims 2-4, 6-8, 10 and 14-16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kean (U.S. Patent No. 7,203,842) and Saito (U.S. Patent No. 6,857,003).

Claims 2, 3 are cancelled; Claim 1 (currently amended) is the former Claim 3 plus its base claims.

Claims 6, 7 are cancelled; Claim 5 (currently amended) is the former Claim 7 plus its base claims.

Claim 10 is cancelled; Claim 9 (currently amended) is the former Claim 10 plus its base claim.

First, a prima facie case for a 103(a) rejection has been claimed but not demonstrated in the Office Action of October 17, 2007. Moreover, there is no incentive to combine the teachings of Kean with Saito. Kean is a FPGA, large digital chip, that does not teach any error correction, whereas, Saito is an analog chip using analog techniques that does teach error correction. Analog and digital techniques as well as chip fabrication are completely separated; the manufacture of FPGA's is completely foreign to an analog, or even a mixed-signal, method of fabrication; and the designers are completely separated, let alone companies which make one or the other are separated. And even if Saito could ever possibly be combined with Kean with future technologies, it is impermissible hindsight and still clearly distinguishable from the teachings of the instant application. Saito is fixated on a 0.5 value so much so that his claims recited "0.5 or about 0.5." Applicants instead wish to detect undesirable random numbers.

Second, Claims 5 (currently amended) and 9 (currently amended), recite root keys and undesirable random numbers not taught or suggested in the references. Finally, Claim 5 is directed to a mobile system, not taught in the references.

Therefore, claims 1, 5, 9 (all currently amended) are believed allowable over the references, along with their respective dependent claims (4, 8, 11).

Claims 14 – 16 being dependent on Claim 12 should also be allowable for at least the same reasons as their base claim.

Respectful request is made for reconsideration of the application, as amended, and for an issuance of a Notice of Allowance. Please charge any missing fees to the deposit account 20-0668.

Respectfully submitted,

/Dolly Y. Wu/
Dolly Y. Wu
Reg. No. 59,192
Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, Texas 75265
972-917-4144